Stimulus-Artifact Elimination in a Multi-Electrode System

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***Abstract*—To fully exploit the recording capabilities provided by current and future generations of multi-electrode arrays, some means to eliminate the residual charge and subsequent artifacts generated by stimulation protocols is required. Custom electronics can be used to achieve such goals, and by making them scalable, a large number of electrodes can be accessed in an experiment. In this work, we present a system built around a custom 16-channel IC that can stimulate and record, within 3 ms of the stimulus, on the *stimulating* channel, and within 500 μs on adjacent channels. This effectiveness is achieved by directly discharging the electrode through a novel feedback scheme, and by shaping such feedback to optimize electrode behavior. We characterize the different features of the system that makes such performance possible and present biological data that show the system in operation. To enable this characterization, we present a framework for measuring, classifying, and understanding the multiple sources of stimulus artifacts. This framework facilitates comparisons between artifact elimination methodologies and enables future artifact studies.**

***Index Terms*—Integrated circuits (IC), multi-electrode array (MEA), neural recording, neural stimulation, stimulation artifact, μNIS, aVLSI.**

I. Introduction

EXTRACELLULAR electrodes are a common tool for the recording and stimulation of electrically active tissue, with applications that go beyond the laboratory into medical implantable devices from pacemakers to deep brain stimulators. Biological neural tissue, and especially mammalian brains, possesses very large neural densities. To extract meaningful information from these networks, large electrode counts are required. In general the need to gain access to large neural populations has made multi-electrode arrays ubiquitous in neural research fields [1]–[3]. Such is the case for some of the ambitious brain–computer interfacing efforts for prosthetic applications [4], [5], *in vivo* applications [6]–[8], and *in vitro* applications such as our Micro Neural Interfacing System (μNIS) effort in the development of 3-D *in vitro* neural models [9]–[11].

Microscale technologies have facilitated the commercialization of multi-electrode arrays (MEAs) that incorporate hundreds of electrodes [12]. Most existing commercial systems [Multi-Channel Systems (MCS), Plexon, Cyberkinetics, etc.], however, still use discrete components for the ancillary amplification and interfacing circuitry; this choice makes the transition to larger electrode counts cumbersome and costly. Several companies and researchers are addressing this problem by developing integrated circuits (ICs) with relatively large channel counts; these ICs reduce costs and facilitate significant size reductions for the interfacing hardware [8], [13]–[19].

Another problem, which has troubled electrophysiologists since early stimulation experiments, is the introduction of stimulation artifacts that obscure any neural activity near the stimulation site for tens or hundreds of milliseconds [20]. The stored electrode charge, which ultimately generates the artifact, introduces problems for long-term stimulation protocols, as it could cause ion migration or general recording system saturation. Although several investigators have tried to cancel the artifact after it has occurred [21], [22], and some groups have tried to eliminate it altogether [23], [24], there is little understanding of the artifact process and properties.

In the present work we describe and characterize a stimulation, recording, and artifact elimination system (Fig. 1) developed around our custom ICs. Our artifact elimination system is built around a second-generation IC (Fig. 2) that introduces improvements in noise performance and stimulation circuitry with respect to the one described in [15]. This system was developed as part of a larger collaboration for the development of *in-vitro* 3-D neural systems under a Bioengineering Research Partnership grant.

II. Stimulation Artifacts

Although further investigation is required to completely describe the stimulation artifact, we will present an overview of the principal factors that are relevant to this work. We focus on the use of a linear *RC* model of the electrode as a first-order approximation to the problem. In order to help standardize the study of stimulation artifacts and the factors that influence them, we provide our definitions while differentiating among the multiple possible artifact sources.

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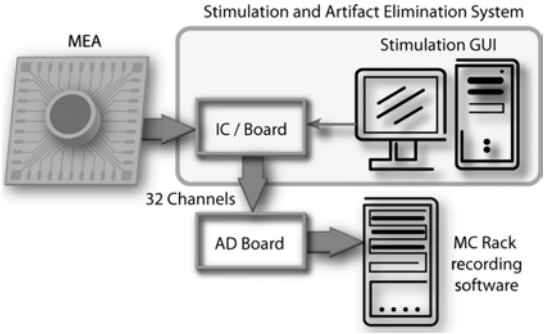

Fig. 1. Biological interfacing system. The MEA is connected by means of an MCS preamplifier plate (being used passively as an interface). See Fig. 6 for a high-level schematic of the stimulation board. In the IC testing setup, Matlab and other instrumentation are used instead of the MCS hardware and software.

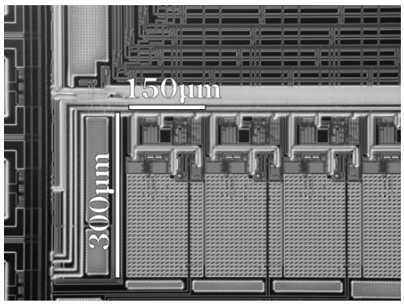

Fig. 2. Photomicrograph of a section of the IC showing 3 of its 16 channels and their associated support circuitry. The largest visible structures are the 16.3 pF input capacitors. Note that less than 25% of the available IC area (of 2 mm × 2 mm) is currently being used.

A. Artifact Origin

The stimulation artifact is a direct consequence of the accumulated charge in the electrode–electrolyte interface during stimulation and of the effect that this charge has on the signal-chain filters and other elements after stimulation [25]. The problem is one of relative scales: stimulation signals are on the order of hundreds of millivolts, while recorded signals are on the order of tens of microvolts (which requires noise levels on the order of a few microvolts). Assuming that charge balancing is made part of the stimulation protocol, very small mismatches of 1% or less, which are common and acceptable in traditional circuit and analog signal processing designs, generate artifacts that would saturate the signal acquisition chain in extracellular recordings. The problem is further complicated by the redox reactions that take place at the electrode–electrolyte interface and make charge balancing difficult to accomplish. If no attempt at charge balancing is made, such saturation would be even more pronounced and longer lasting.

To allow the recording of signals after stimulation, the charge on the stimulating electrode has to be dissipated to a level that allows for the normal operation of the amplification circuitry. For typical stimulation protocols, in which a residual voltage of 200 mV or more can be left in the electrode, to completely eliminate the artifact (i.e., to bring the residual voltage down to the electrode noise level) the electrode charge has to be dissipated to one part in 100 000 or better. To be able to recover the signal, with a typical signal amplification chain that would

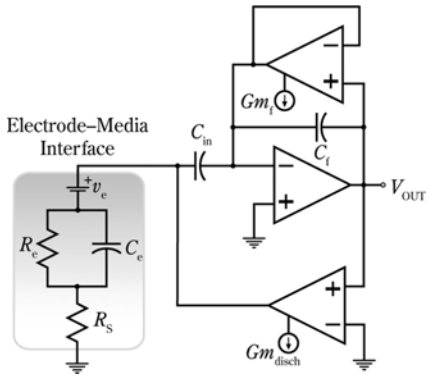

Fig. 3. IC discharge circuitry, notice that the main amplifier is part of the discharge loop and it is responsible for storing the electrode dc voltage. $G_{\mathrm{m_{disch}}}$ is the transconductance (bias) of the discharge amplifier, $G_{\mathrm{m_f}}$ the transconductance (bias) of the feedback amplifier (which sets the highpass pole frequency), R_{e} and C_{e} are the equivalent electrode resistance and capacitance, R_{S} the spreading resistance, and v_{e} the electrochemical potential.

saturate at about 2 mV, the residual electrode charge has to be dissipated to one part in a hundred or better. Using the linear electrode model shown in Fig. 3 [26] and the exponential decay of the electrode charge that such a model predicts, we need to let five time constants of the electrode elapse to recover the signal; to eliminate the artifact (i.e., dissipate the charge to one part in 100 000), at least eleven time constants would have to elapse. For a 40 μm × 40 μm platinum black extracellular electrode in an open circuit (i.e., connected only to high impedance recording circuitry), with a time constant ($R_{\mathrm{e}}C_{\mathrm{e}}$ in Fig. 3) of 10 ms, this can be from 50 to 110 ms. Clearly, these times are too long to enable the measurement of direct responses to stimulation; furthermore, unbalanced stimulation protocols can extend the artifact duration into the tens of seconds.

A way to reduce the artifact duration would be to reduce the electrode discharge time constant, which can be achieved by connecting the electrode to its poststimulation stabilization voltage through a low impedance path. Such a connection would reduce the time constant from the 10 ms of our previous example to approximately 200 μs ($R_{\mathrm{S}}C_{\mathrm{e}}$ in Fig. 3), a 50-fold reduction. Such reduction would translate into artifacts that enter the linear range of the recording circuitry in 1 ms and an artifact that enters the noise band in 2.2 ms; durations that are commensurate to the expected neural response times. Because the electrode poststimulation voltage is not necessarily known in advance, the electrode prestimulation voltage can be used as a reasonable approximation.

The long-lasting artifact dependencies and nonlinear processes that result from redox reactions at the electrode–electrolyte interface are not captured by the linear electrode model; the interaction of these factors with the stimulation signal would be seen as temporary changes in the linearized electrode characteristics which could translate into additional artifact problems. Although more elaborate electrode models are readily available [27], [28], the linear model is sufficient to approximate most of the artifact behavior and, because of our use of continuous feedback, the behavior of the circuitry itself [25].

It is worth pointing out that most existing designs attempt to cancel the artifact from the signal chain after it has been produced (the main exception being [23]). Our design seeks to eliminate the artifact from the electrode itself. Additionally, our design, by placing the electrode in a feedback loop and allowing for the continuous variation of system parameters, should be able to compensate for factors (e.g., nonlinearities in the electrode) that the existing, feed-forward, designs are not able to address.

B. Artifact Duration

Given the nature of the discharge behavior, it is not really possible to specify objectively the point at which the artifact has dissipated because some long-lasting baseline shifts might be introduced; these shifts are at least partially due to electrode nonlinearities and can vary with the electrochemical environment and the stimulation history. Requiring the remaining artifact voltage to become comparable to the recording noise level after stimulation would be overly conservative for most applications and could introduce data artifacts due to dependance on the slow components of the phenomena that we are trying to measure.

With regard to the recording range of the system (or, more restrictively, the linear range of the recording system) we can classify stimulation artifacts as *nonsaturating* or *saturating*. As long as the signal chain (i.e., all amplifiers and other elements in the recording path) is not saturated or overly distorted, the artifact can be eliminated using signal processing methods (SALPA [29], filtering, etc.). Such processing would be required before postprocessing algorithms, such as spike detection or spike sorting, can be applied to the signal. If the signal chain saturates, any signal present in that interval is lost and no amount of signal processing will be able to recover it, this saturating artifact, is what must be eliminated or at least reduced as much as possible. This saturating artifact is what traditionally makes recording impossible for tens or hundreds of milliseconds after stimulation.

To be able to make the distinction between nonsaturating and saturating stimulation artifacts, the whole signal chain must be taken into account; gains, filters, amplifiers, digital converter resolution, and all voltage ranges have to be considered (which will be different for each system and setup). Given typical resolutions and extracellular signal magnitudes for MEAs, ranges of approximately 2 mV are common. For the purpose of this paper, we chose to define *artifact duration* as the time from the end of stimulation to the time that the recording system returns to within 200 μV of the electrode voltage *before* stimulation. Although this value is a poor choice in terms of promoting our technology, such conservative threshold allows for a direct comparison between very different systems; and it enables a signal to be observed, without any additional processing, on top of the remaining artifact.

C. Artifacts Resulting From Circuit Effects

Although the primary cause of stimulation artifacts is the charge stored in the electrode, the artifact can be aggravated by effects from the intervening circuitry. These effects are generally avoidable through careful circuit design and layout. Here we highlight how our system deals with circuit effects.

1) DC Rejection Passband: Among the circuit effects, the highpass characteristics of the dc rejection filters in the recording circuitry can be the largest contributors to the stimulation artifact. When the system returns to recording mode, the transition caused by the stimulation-induced electrode offsets (and other offsets) will excite such filters. This voltage step can generate long-lasting and large magnitude effects. The best way to avoid this problem is to eliminate the charge-induced offset, before the signal reaches the filters in the recording path; this approach, however, is not always possible or convenient. An alternative is to use first order high pass elements and the highest highpass frequency acceptable for the application (which restricts the duration of such effects). Satisfying the conflicting requirements of signal bandwidth and artifact reduction can lead to undesirable compromises; we have avoided this tradeoff by varying the filter poles during artifact elimination (see Section III-D).

2) Charge Injection: Many early artifact suppression schemes were hampered by switching element charge injection [30], which is magnified by the required amplifier sensitivity. To reduce some of these effects, some designers amplify and limit the signal before introducing switching elements, thus limiting the introduced transients (e.g., the MCS MEA1060-BC preamplifiers and [23]). Our designs avoid this problem altogether by making all charge injection paths into common mode current bias paths [15]; that way, the existing common mode attenuation of differential amplifiers and the low impedance of the involved nodes drastically reduce any effects due to charge injection.

3) Circuit Mismatch: If we dynamically insert and remove elements from the signal path, or actively modify the characteristics of the elements themselves, any common-mode mismatch problem will cause transients on element switching. In our own design, due to the extremely low biases required, changing the highpass filter cutoff frequency introduces a mismatch transient that is a function of the filter's bias currents. The same is true for the interaction of the discharge path bias current with the electrode impedance and the remaining electrode charge. These mismatches can cause transients which might look similar to those generated by charge injection. A time-consuming circuitry redesign will inevitably face diminishing returns as such mismatches would be unavoidable without additional offset trimming [31] and it is physically impossible to alter the electrode discharge path interaction. Slowly changing any variable that is known to induce mismatch-related artifacts provides an alternative to reduce the transients caused by these phenomena. Our current firmware implementation can make use of this technique for the discharge path current.

4) Crosstalk: In any system with multiple channels in close proximity, signals can interfere with each other, a phenomenon known as *crosstalk*, *signal coupling*, or *feed-through*, depending on context. In a mixed-mode system (analog and digital), or in other systems in which large magnitude signals are present alongside small signals and amplification elements, the crosstalk problem can become more severe. For example, stimulation signals due to their large magnitude can introduce

TABLE I
MAIN CHANGES TO IC SPECIFICATIONS FROM THOSE OF [15]

Parameter	This work	[15]
Main amplifier bias	25 μA	13 μA
IC gain	100 $^{\mathrm{V}}/_{\mathrm{V}}$	48 $^{\mathrm{V}}/_{\mathrm{V}}$
$C_{\mathrm{I}}/C_{\mathrm{F}}$	8 pF/40 fF	2 pF/40 fF
Input referred noise (200 Hz-3 KHz)	3 $\mu\mathrm{V}_{\mathrm{RMS}}$	4.4 $\mu\mathrm{V}_{\mathrm{RMS}}$
Maximum stimulation current	$\pm$100 μA	$\approx \pm 10\,\mu\mathrm{A}$ [a,b]
Maximum stimulation voltage	$\pm$1.3 V	$\approx \pm 1.5$ V [a]

[a] Design oversights required the addition of external components.
[b] Available current changed exponentially with stimulation voltage.

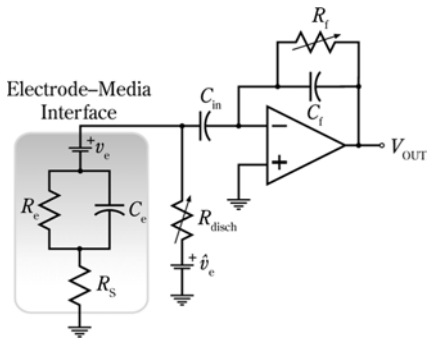

Fig. 4. Equivalent discharge circuitry disregarding the frequency response and saturation characteristics of the amplifiers. $\hat{v}_{\mathrm{e}}$ is the lowpass estimate of the electrochemical potential, and $R_{\mathrm{f}} = (1/G_{\mathrm{m_f}})$ allows the tuning of the dc-blocking frequency.

crosstalk into adjacent channels. This effect can be reduced through careful layout techniques or by adding design elements to increase the electrical separation between signals. Although our system can reduce external coupling to recording channels by providing a low-impedance path during stimulation, our current design has some layout oversights that introduce additional crosstalk problems (see Section V-A.3 and Fig. 15).

III. IC DESIGN

The focus of this paper is on the design of the system built around our second generation 16 channel stimulation, artifact elimination, and recording IC and the evaluation of the system for its intended biological application. Most of the details of the design of the IC have been presented previously [15], the main design changes can be seen in Table I. In this section, we highlight the improvements with respect to the previous design and expand on details that are relevant to this work.

A. Artifact Elimination

The artifact elimination circuitry was described previously [15]; for ease of reference we reproduce the circuitry during the discharge phase in Fig. 3, and an equivalent circuit model (valid for most of the discharge when the circuitry is out of saturation) can be seen in Fig. 4. As the equivalent model indicates, and given the subthreshold circuit elements, the discharge phase is roughly equivalent to connecting the electrode, through a controllable resistor given by

$$R_{\mathrm{disch}} \approx \frac{1}{A_{\mathrm{V}}\, G_{\mathrm{m_{disch}}}} = \frac{U_{\mathrm{T}}}{A_{\mathrm{V}}\, I_{\mathrm{disch}}} \approx \frac{26\,\mathrm{mV}}{200\, I_{\mathrm{disch}}} \qquad (1)$$

to the prestimulation average electrode dc voltage ($A_{\mathrm{V}} = 200$ is the main amplifier gain and $U_{\mathrm{T}} \approx 26$ mV is the thermal voltage). With a maximum discharge current of approximately 100 μA, the minimum R_{disch} will be on the order of 1.5 Ω. From this circuit, and assuming polarizable electrodes for which $R_{\mathrm{e}} \gg R_{\mathrm{S}}$, it can be shown that the discharge phase will have a time constant on the order of $(R_{\mathrm{S}} + R_{\mathrm{disch}}) \times C_e$. With this equivalent circuit, for the electrode capacitance to discharge from $V_{\mathrm{C_e}0}$—the electrode voltage at the end of stimulation—to a level of $V_{\mathrm{C_e}d}$—either inside recording range or any other arbitrary level—it will take

$$t_{\mathrm{disch}} \approx (R_{\mathrm{S}} + R_{\mathrm{disch}}) C_{\mathrm{e}} \times \ln\left(\frac{V_{\mathrm{C_e}0}}{V_{\mathrm{C_e}d}}\right). \qquad (2)$$

With this linear model, a 220 mV residual voltage in C_e will take ten time constants to discharge to 10 μV. A similar equation describes the discharge time for an open electrode; in this case, the time constant becomes approximately $R_e \times C_e$, which in general can be two or more orders of magnitude longer than the one allowed by our circuitry.

Keep in mind that, besides a dependency on the involved ionic species and concentrations, R_S is inversely proportional to the electrode geometrical area while R_e and C_e depend on the active electrode surface area and material [28]. Therefore, all these factors will be dependent on the specific electrode and electrode conditions. Given the above, every electrode will have its own artifact characteristics, even more so if we consider the many time variant, nonlinear, and stochastic effects brought about by surface interactions with ionic species.

We can see from the equivalent circuit of Fig. 4 that R_{e}, R_{S}, and R_{disch} constitute a voltage divider for the charge remaining in the electrode capacitance (C_{e}). As R_{disch} depends on the discharge current (I_{disch}) through (1), if the electrode capacitance (C_{e}) is not fully discharged, any changes on the discharge current will cause a voltage transition at the input of the amplifier. To reduce this effect, the system firmware was designed to follow a parameterized discharge curve that guarantees that at the end of the transition the discharge amplifier bias current temporal derivative, and thus the discharge impedance derivative, is zero $(\partial I_{\mathrm{disch}}/\partial t = 0 \rightarrow \partial R_{\mathrm{disch}}/\partial t = 0)$. The firmware thus implements two sets of *discharge phases* joined by such smooth transition.

B. Stimulation Buffer

The stimulation buffer, presented previously [15], had a significant current limitation due to its bias network. The biasing complexities of the circuit and the operating range of the design prompted us to simplify the circuitry (allowing for additional functionality). The new stimulator (Fig. 5) is a simple operational transconductance amplifier (OTA) in a follower configuration in which input signals and bias currents are switched between stimulation levels. This configuration allows for the application of an arbitrary externally generated stimulation waveform or for the use of current stimulation under some bias and electrode conditions (if the OTA's inputs differ by more than approximately 100 mV, it would behave as a constant current source). This circuitry can provide close to 100 μA on a $\pm$1V stimulus, which is more than enough for most cell-culture MEA applications [32]. The stimulation voltage, and ultimately the

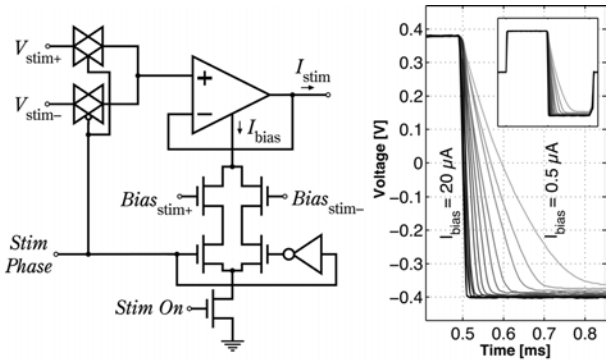

Fig. 5. Re-designed stimulation buffer. Note that it provides two different maximum currents depending on the stimulation phase input. The graph shows the use of the current adjustment feature on an MCS reference *RC* electrode.

stimulation current for a given electrode impedance, is limited by the IC supply, which is of ± 1.65 V for the 0.35-μm TSMC IC technology used.

C. Recording Noise

As reported in [15], the noise level of our previous design was larger than expected; furthermore, subsequent evaluation revealed that the design noise specifications had to be further reduced. To overcome this problem without greatly increasing the amplifier size (or a risky redesign), a simple solution was carried out, which implied an increase of the voltage gain of the recording amplifier to 200 (from 50) by increasing its input capacitance (C_{I}) by a factor of four, and increasing its bias current by a factor of two. Both of which, by the relation [15, eq. (8)]

$$\overline{v_{\mathrm{ni}}^2} = \frac{(C_{\mathrm{F}}+C_{\mathrm{I}})^2}{{C_{\mathrm{I}}}^2}\frac{16\,kT}{3\,g_m}(3\ \mathrm{kHz}-30\ \mathrm{Hz}) + \frac{C_{\mathrm{F}}}{{C_{\mathrm{I}}}^2}\frac{32\,k\,T}{6\,\pi}\left[\frac{f_{\mathrm{HP}}}{f_{\mathrm{HP}}+30\ \mathrm{Hz}}-\frac{f_{\mathrm{HP}}}{f_{\mathrm{HP}}+3\ \mathrm{kHz}}\right]. \quad (3)$$

should reduce the overall noise by a factor of four. To accommodate such an increase in gain without affecting the amplifier bandwidth, we had to add an output buffer to each stage (following the design in Manetakis [33]), which due to its 6 dB loss reduced the overall IC gain to 100. This addition introduced some crosstalk that reduced the performance of adjacent channels, probably due to power supply coupling.

D. Pole Shifting

Given that part of the stimulation artifact is due to the filter response of the recording circuitry, a recent work by DeMichele and Troyk [21] and some testing with our previous generation IC suggest the implementation of a temporary recording bandwidth modification, or *pole shifting*—that is, increasing the recording highpass pole in the stimulating channel to increase the recovery speed of the amplifiers. Given that we have dynamic control over the highpass pole of our main amplifier (through $G_{\mathrm{m_f}}$), a separate bias path can be used to selectively alter recovery speed. By adding three transistors in the bias branch of the feedback amplifier, and one additional control bit and bias input, we can increase the highpass poles only of selected channels. The firmware makes use of this feature by adding a set of pole shifting phases after the discharge phases.

E. IC Controls

As a test design, the control of the multiple digital features of the IC was implemented through simple 16-bit latched shift registers, using one bit per channel. Each one of the five digital variables has its own dedicated shift-register, namely: Amplifier activation, pole shifting, stimulation buffer activation, stimulation phase, and discharge buffer activation.

Additionally, there are eight analog values to be controlled: highpass pole frequency, highpass pole shift frequency, stimulation high and low levels, stimulation high and low currents, discharge bias current, and amplifier reference level. Several of these analog input variables include resistive dividers that serve to increase the usable resolution of the external drive voltages while keeping the internal voltage inside a reasonable range. An external resistor, in combination with internal reference circuitry, sets the main amplifier bias current (25 μA).

IV. System Design

The test system consists of a custom board, depicted in Fig. 6, with an isolated power supply for the circuitry, a PIC microcontroller (Microchip 18LF452) running at 30 MHz, twelve 12-bit digital to analog converter (DAC) channels (three Analog Devices DAC8420 ICs with four channels each), 32 discrete operational amplifiers (eight Texas Instruments LF347 with 2% 10 KΩ and 270 Ω Bourns 4816P-1 feedback resistors for a gain of 38 v/v) to buffer and further amplify the recorded signal level, and two of our custom analog VLSI ICs. The ICs and the DACs share the same 7.5-MHz serial interface (SPI/Microwire) to the microcontroller, and the board communicates with the computer through an optically isolated RS-232 serial interface running at 115 200 bits/s. On the computer a custom Matlab (Mathworks) graphical user interface, or custom Matlab functions, are used to format and send configuration information to the board or to trigger a stimulus sequence. For the system tests, the board inputs are connected directly to a multi-electrode array; the amplified outputs are connected to an analog interface card (National Instruments 6035E), which also receives triggering signals from the board. For the biological tests the analog outputs from the board are sent to a MCS A/D board, and the inputs are connected in parallel with an MCS preamplifier box (MEA 1060) to a MEA with the neural cell culture, which allows the simultaneous measurement of signals through both systems.

The microcontroller firmware is programmed to sequence the signals for the ICs, so that the different biases are present, and the required circuit elements are turned on and off in the different recording, stimulation, and discharge phases. Switching in between phases can take 40 μs or less, depending on the number of signals to be changed and other firmware requirements. The overall timing resolution and jitter of the system is on the order of 600 ns or less, though the interface requirements restricts timing to 10 μs increments (firmware calibration constants are used to compensate for most delays). An additional optically isolated trigger input to the microcontroller can be used to start a stimulation sequence. The above system timing limitations are caused by our current choice of interface (both to the firmware and to the IC). Future implementations can eliminate all of these limitations by firmware modifications, the use of dedicated custom digital hardware, and ultimately by redesigning the IC digital interface.

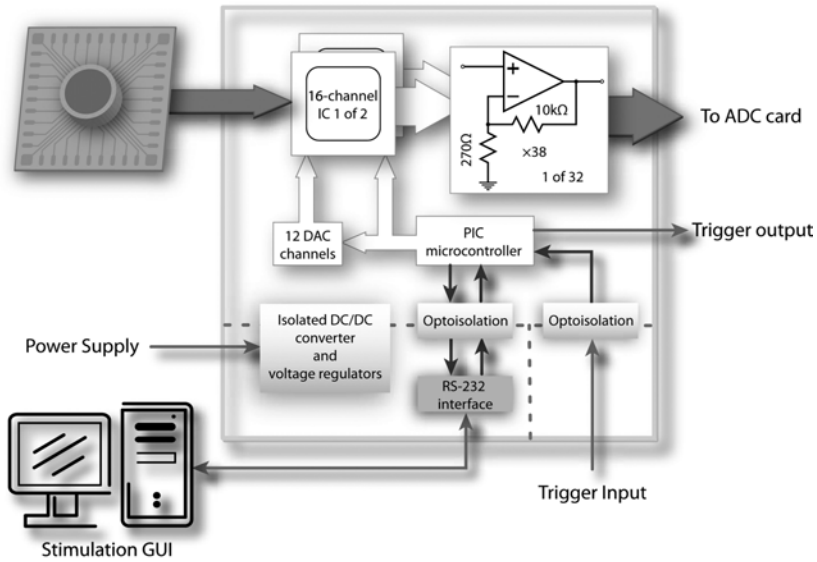

Fig. 6. High-level system schematic. The board includes two of our VLSI ICs and additional interfacing circuitry. For most tests only the channels under consideration were connected to data acquisition hardware.

V. Results

We have characterized the artifact elimination system, and demonstrated the validity of the custom aVLSI circuitry and its ancillary board in a real neural stimulation and recording application. As artifact elimination performance is the main distinguishing feature of this work, we have concentrated our efforts on evaluating this aspect of our design and methods (although, for completeness, we start this section with some basic amplifier characterization data).

A. IC Characterization

To characterize the performance of the IC recording path, a Stanford Research Systems SR785 dynamic signal analyzer was successively connected to each channel under identical bias conditions, and the whole board gain, bandwidth and noise characteristics were measured in all 16 of the IC channels.

1) Channel Uniformity: In Fig. 7, the average response for a highpass filter setting of 10 Hz shows that at 500 Hz, an average gain of 3195, with a standard deviation of 26, was obtained (that is, 70 $\pm$0.07 dB), with a flatness of $\pm$0.5 dB in the 100 Hz–1 kHz range. The average lowpass cutoff for all 16 channels was 3348 Hz, with a standard deviation of 80 Hz. Although no specific effort was placed into matching the different channels, these results highlight the advantages of a monolithic construction. Note, however, the high variance in the highpass poles of the different channels; such variance could be partially due to the extremely low bias currents that are being used in this filter stage (on the order of 1 fA), which are comparable to leakage currents in the circuitry. The fact that the variance appears constant in a logarithmic scale at different filter settings ($\sigma = 4$ Hz at 10 Hz and $\sigma = 50$ Hz at 100 Hz), however, suggests a mismatch in the bias circuitry of the filter amplifiers. Because this part of the design was mainly intended for dc rejection and in many of our experiments we filter downstream with a highpass filter at 200 Hz, this effect is not problematic for our current application.

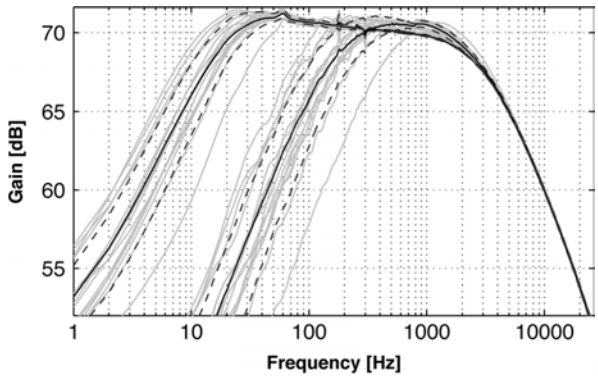

Fig. 7. Gain and bandwidth matching for the 16 recording channels in an IC at highpass pole settings of 10 and 100 Hz. The dark traces show the average transfer function with dashed lines that represent $\pm 1\sigma$ from the mean, the light traces are the 16 individual channel responses.

2) Input Referred Noise: From Fig. 8, we can see that for a functional highpass setting of 10 Hz, the RMS noise in the 200 Hz–3 kHz bandwidth of interest is of 3.0 μV ($\sigma = 1.28\,\mu$V), which is lower than our previous IC (by 1.4 μV). Additionally, the noise dependance on the bandwidth of the amplifier was reduced with respect to that of [15]. Although the noise level is part of the design decision that seeks to develop the smallest reasonable IC implementation and the lowest bias currents, the noise is still larger than expected and the noise reduction is smaller than expected. A likely source of the extra noise is the output buffer coupled with low power supply rejection in the preamplifiers, but at this point we cannot discard the influence of other circuit elements (e.g., pad protection diodes, stimulation buffer, discharge amplifier, or $1/f$ noise in the feedback path or the main amplifier).

According to specifications, our noise is still three times that of the MCS MEA-1060 amplifier. To evaluate our noise figure,

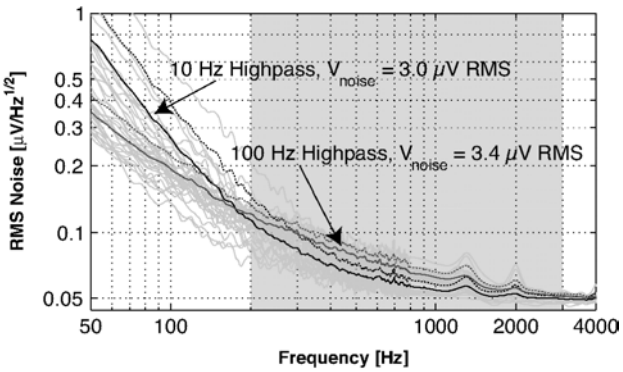

Fig. 8. Input referred noise of the 16 recording channels in the IC for a 10 Hz and a 100 Hz filter setting. The dark traces show the average noise density of all channels with the dashed lines representing $+1\sigma$ from the mean, the light traces are the individual channel noise. The gray region is the frequency band for which the RMS noise values were calculated. (RMS noise values had $\sigma = 1.28\,\mu$V at a 10 Hz highpass and $\sigma = 1.22\,\mu$V at 100 Hz).

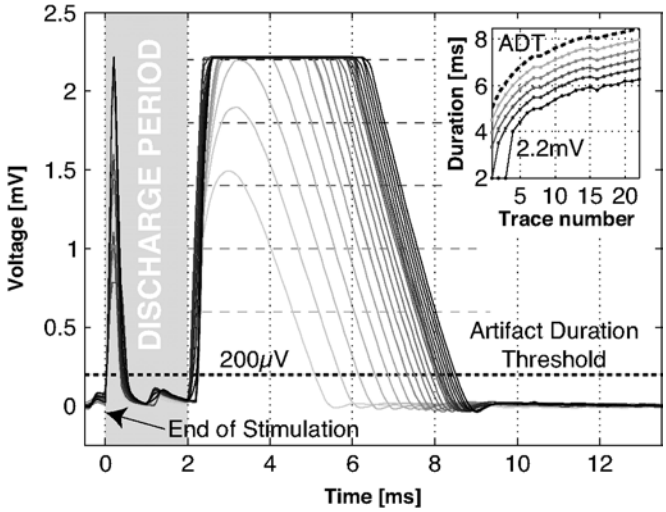

Fig. 9. Example of the output of the recording system after a ± 500 mV, 200 μs per phase stimulation and a 2-ms discharge (not enough to eliminate the artifact). In this figure, as in all subsequent figures, $\mathrm{time} = 0$ indicates the end of stimulation and the beginning of electrode discharge. The main amplifier is active at $t > 0$ (and off during stimulation), the discharge amplifier is active only during the discharge period. This 25 trace recording is a transient behavior at the initiation of 8 Hz periodic stimulation (darker traces happened later in time). The artifact variability can be seen to converge towards a narrow range of values. The initial spike (as the main amplifier is turned on), and the relatively flat region that follows, is due to the activity of the discharge loop. In this case, the recording system saturates at approximately 2.25 mV. The inset shows the artifact duration depending on the chosen threshold (the shading corresponds to the thresholds indicated by dashed lines in the main figure). An artifact duration threshold (ADT) of 200 μV was chosen for this work.

we compared our IC to the MEA-1060 connected to an active MEA under the same conditions and recording information from the same culture (see Section V-C.1). Defining SNR as peak recorded neural spike value divided by the RMS noise of the channel and averaging across 6 active electrode channels, we found that the MCS amplifier provided an SNR of 12.8 ($\sigma = 3.0$), while our system one of 8.7 ($\sigma = 1.4$). That is, in our particular experimental setting, our SNR is comparable to that of the MCS amplifier (approximately 3 dB worse), as a significant part of the noise comes from the electrode.

3) Crosstalk: The present IC design has some layout oversights, mostly due to the addition of output buffers, that substantially increased the crosstalk in between channels in comparison with our previous-generation IC. Such crosstalk is particularly problematic during stimulation, given that it introduces artifacts in the recording path of adjacent nonstimulating channels. Although this is only noticeable thanks to our artifact removal architecture, we reduced this problem by modifying our stimulation protocol, turning off nonstimulating channels during the presence of the largest offending signals, namely stimulation and the initial phase of electrode discharge; we also have the possibility of activating the discharge circuitry on the recording electrodes during the stimulation phase.

B. Artifact Behavior

To validate the circuitry, a 40 μm $\times$ 40 μm array (Ayanda Biosystems) was plated with platinum black to a uniform impedance of 20 kΩ at 1 kHz using the aparatus described in [34]. The array was submerged in Hank's balanced salt solution, 16 of its 60 electrodes were connected to our IC, and an additional ground wire electrode was placed in the media. In all the experiments in this section, a $\pm$500-mV, 20-μA maximum stimulation current, 200 μs per phase, positive-first, biphasic voltage stimulus was used. Unless otherwise indicated, the highpass pole of the input stage was set to 200 Hz. Artifact data were captured at a constant stimulus repetition rate of 8 Hz, and at least 25 full stimulation–cancellation cycles preceded the captured data, which, as seen in Fig. 9, was roughly enough for the fastest components of the initial electrode 'accommodation' transients to die out (such transients are probably due to changes in the equilibrium between reduction and oxidation of chemical species at the electrode site [35]). The artifact magnitude and polarity were a consequence of the stimulus being used and the main amplifier's 180° phase shift. Additional discharge cycles in between measurement sequences were used to avoid excessive charge accumulation (and electrode damage) for suboptimal discharge parameters. After the accommodation period (25 stimulation–cancellation cycles), five additional stimulation cycles were captured and averaged to obtain a single trace. These data capture conditions insured that, after an initial transient that is dependent on previous electrode conditions, the traces would settle with relatively small variations (and slow time constants). We have observed the artifact continue to drift in different directions, in no discernible pattern, for more than 24 h, which implies an underlying stochastic process.

It is worth noting that, as a consequence of the design, the actual discharge current will be determined by the charge and voltage of the electrode itself; that said, for all discharge settings in this paper, as we use a symmetric biphasic voltage stimulus, the current to the electrode will have three phases: 1) a "precharge" (anodic) phase in which the electrode voltage is raised, thus increasing the available current for the next phase; 2) a "stimulation" (cathodic) phase in which the transition to a negative voltage generates the stimulation current in the MEA [32], which charges the electrode to a negative voltage (such symmetry in voltage causes asymmetry in current and charge); and finally, 3) a decaying anodic discharge current to drive the electrode to its resting potential, which will be present in the

media and could affect neural response [35]. It is important to keep in mind that for some stimulation protocols the constraints on discharge current might impose some additional performance limitations; likewise, the use of different stimulation protocols (e.g., charge-balanced current or voltage stimulation) will improve on the reported performance.

1) Artifact Duration: The recording range present in Fig. 9 ($\approx$2.25 mV above the prestimulation baseline) is a consequence of our power supply, gain, digitizer, and offset settings, but the recording ranges can be deemed arbitrary for most purposes. As we have already mentioned, for consistency we chose 200 μV as our *artifact duration threshold*, and the artifact duration data reflect that choice. In cases where the artifact does not exceed the artifact duration threshold, the discharge time (during which no recording is possible) will be used instead.

To show the meaning of the measures presented in subsequent figures, the data traces in Fig. 9 are presented alongside several artifact duration measurement thresholds, and the inset shows the effect of the choice of threshold on the final measurement. Note that the relation between the voltage threshold and the artifact duration is roughly linear, and that our choice of a lower threshold imposes a penalty of two to five milliseconds over a higher threshold that accounts for the recording range.

2) Discharge Current and Time: For clarity, and as a consequence of our design choices, we have divided the discharge process into two discharge periods. The initial one significantly lowers the charge of the electrode, while the second one allows us to better visualize the artifact. Fig. 10 shows the effect of the initial electrode discharge on the artifact duration. At the initiation of discharge, the main amplifier is turned on, and the large electrode offset drives it (and the discharge amplifier) out of its linear range (the initial spike seen in Fig. 9). During these few microseconds the equivalent circuit in Fig. 4 will not be valid, and the discharge rate will be directly proportional to the available discharge current (I_{disch}). It would seem that the larger the discharge current, the smaller the artifact duration, but larger currents also cause large transients at the end of discharge as, unless the electrode is fully discharged, the input of the amplifier will see a voltage step proportional to the change in voltage divider formed by R_{disch} and R_S.

To avoid such transients, a second discharge phase at a lower discharge current can be used to reduce overall discharge time. Fig. 11 shows the effect of the second discharge phase after the application of a 500-μs, 10-μA initial discharge. As expected from (1) and (2), the artifact duration roughly saturates for larger currents as R_S dominates the discharge time constant, though the actual data shows a minimum across time, as larger discharge currents are used. Among other smaller effects, the presence of such minimum will be due to a small offset between the poststimulation electrode resting voltage and the stored average electrode voltage, which causes a voltage step at the end of discharge. Once the electrode is "reasonably" discharged, we will face diminishing returns as recording cannot take place during the discharge period.

3) Soft Switching: As large transients can affect the filter and the electrode itself, we have the option of switching smoothly between discharge values. Fig. 12 shows the effect of a smooth curve that reaches the second discharge phase with a zero time derivative (a voltage parabola distorted by the exponential voltage-to-current relationship of the bias circuitry). Note that

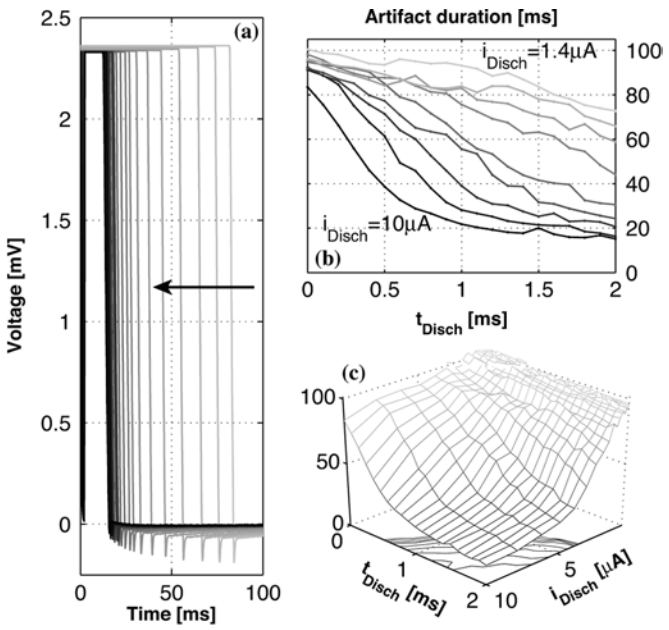

Fig. 10. Artifact duration with respect to discharge current and discharge time. (a) Set of time traces of artifact data after a $\pm$0.5 V, 200 μs per phase stimulus (current limited to 20 μA), with a discharge current of 10 μA parameterized by discharge time (from 0 to 2 ms); the arrow indicates the direction of increasing discharge time. (b) Artifact duration with respect to discharge time parameterized by discharge current (section of logarithmically spaced data set with 20 current traces from 10 to 0.1 μA). (c) 3-D representation of the whole data set from (b). Note that the undisturbed artifact duration is $\approx$100 ms.

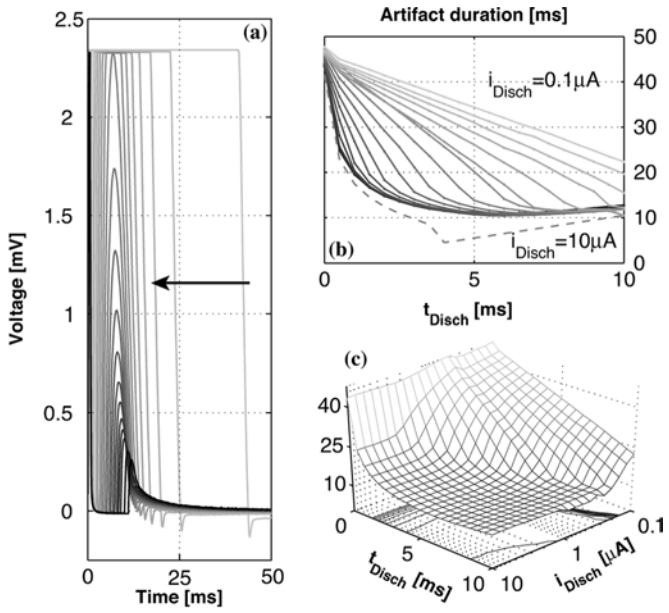

Fig. 11. Artifact duration after an initial discharge period of 500 μs at 10 μA. (a) Set of time traces of artifact data with a discharge current of 10 μA parameterized by discharge time, the arrow indicates the direction of increasing discharge time. (b) Artifact duration with respect to discharge time parameterized by discharge current (logarithmically spaced, 20 current traces from 10 μA to 0.1 μA). The dashed line corresponds to a higher artifact threshold of 2 mV (the sloped region is the total discharge time as the artifact does not exceed the threshold). (c) 3-D representation of the data set from (b). Note that the artifact duration slightly worsens for larger discharge currents and times.

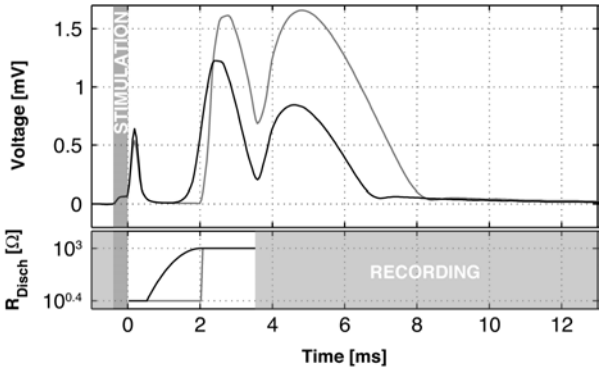

Fig. 12. Example of two artifacts with (black) and without (gray) a soft transition between the high and low discharge currents. The bottom plot shows R_{disch} for each curve; both start and stop at the same values and have a total discharge time of 3.5 ms. The initial peak saturates the amplifiers though the higher currents make it too fast to be captured at this sampling rate. The gray regions denote the areas in which the corresponding amplifiers are turned off. Note that the larger overall current (smaller overall R_{disch} value) performs worse than having a smooth transition.

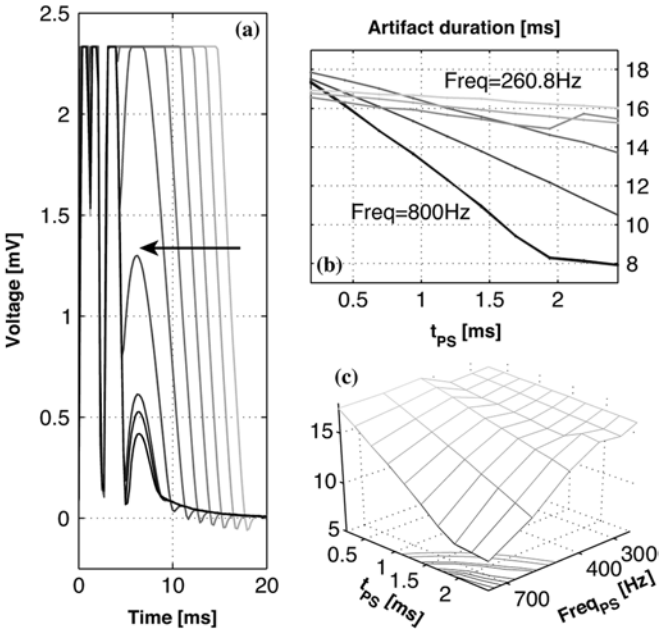

Fig. 13. Artifact duration with respect to pole shift time and frequency after a discharge period of 1 ms at 5 μA, followed by 1.5 ms at 1 μA. The pole-shift effect is additive to the recording highpass frequency of 200 Hz (the frequencies shown are actual highpass values). (a) Set of time traces of artifact data with a pole shift frequency of 800 Hz parameterized by pole shift time, the arrow indicates the direction of increasing pole shift time. (b) Artifact duration with respect to pole shift time, parameterized by pole shift frequency. (c) 3-D representation of the data set from (b).

the artifact duration has been further reduced by approximately 1 ms even though overall discharge time remains the same, the average discharge impedance is higher, and the transition at the end of discharge remains unchanged. Although we are not sure of the mechanism for such artifact reduction—and we found it while implementing a way to continue discharging the electrode during recording—we have found some evidence that the fast transients affect the electrode itself rather than the recording path (see Section V-B.5).

4) Pole Shifting: As was made clear by the design in [21], the frequency characteristics of the amplifier itself contribute to the artifact, so a way to further reduce the artifact duration is to modify the frequency response of the main amplifier for a short time period after discharge. Fig. 13 shows this effect. Due to the way the poles are controlled in our ICs (see Section II-C.3), this method will introduce some artifacts due to switching between offset levels (no soft switching has been implemented for this path yet). As long as the bandwidth is not considerably reduced, this mode of artifact reduction has the advantage that recording can take place during the period of pole shifting (as is also true, though harder to accomplish, for the second discharge phase), but we must keep in mind that the pole shift setting affects the recording chain itself and has no direct effect on the electrode.

5) Remaining Discharge: In Fig. 13(a), we can see an apparently exponential decay after the main artifact—which is present, though not always evident, in the other figures—this decay has roughly a 4.4-ms time constant, which is slower than any time constant on the electronics path thus pointing to the electrode as the most likely source. All the curves reach the same exponential decay, which is to be expected as pole shifting only changes the recording path and not the electrode. From Fig. 12 a time constant of 4.8 ms can be extracted (which is within measurement error from the previous value), although interestingly the soft-switch curve is roughly 12 μV below the abrupt switching curve, which strongly suggests that the electrode itself is being affected by the speed of the transition.

Extracting time constants from the data in the other discharge curves (Figs. 10 and 11), we find that their values are not consistent, ranging from 15 down to 5 ms (and many of the traces have sign-inversion which suggests over-discharge). These measurements highlight some of the limitations of the linear model, as such variation cannot be explained with constant capacitance and resistance values. Nonetheless, the time constants are in the right order of magnitude, as required by the *RC* model of the electrode (approximately 10 ms). Interestingly, there seems to be a relationship between how fast the remaining artifact decays and how fast the discharge is, so that an undischarged electrode would generate not only the longest but also the slowest decaying artifact.

C. Biological Tests

1) Methods: Dissociated E18 hippocampal neurons (Brain Bits[1]) were plated on an MEA (30 μm TiN electrodes with Si3N4 insulator, MCS, Reutlingen, Germany) with serum-free Neurobasal medium (Gibco) with 2% B27 (Gibco), 0.5 mM L-glutamine (Gibco), 25 μM glutamate and 0.1% penicillin-streptomycin (Sigma-Aldrich). MEAs were incubated at 37 °C, 5% CO_2, and 9% O_2, and biological experiments were done at the fourth week after the plating. The MEA was connected into the rest of the system as indicated in Section IV. All animal procedures were done in accordance with approved animal use protocols at the University of Illinois.

2) Results: Cultured hippocampal neurons were spontaneously active, and synchronized bursting activity could be routinely recorded through our IC. As indicated in Section V-A.2

[1]www.BrainBitsLLC.com

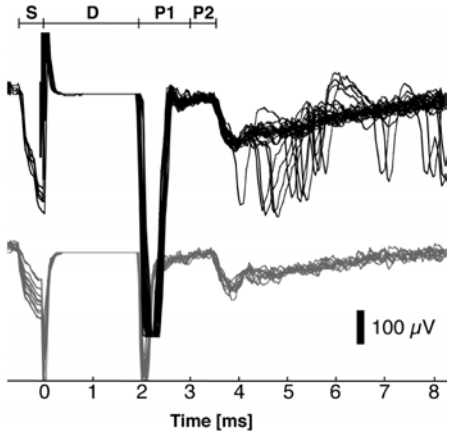

Fig. 14. Recordings from the stimulating electrode with a discharge time (D) of 2 ms @ 50 μA, two pole-shift phases of 1 ms @ 2200 Hz (P1) and 0.5 ms @ 700 Hz (P2). Highpass filter setting: 200 Hz. Stimuli (S) were positive-first biphasic pulses (pulsewidth 200 μs for each phase) with an amplitude of 0.1 V (bottom trace) or 0.5 V (top trace). Note the recorded responses starting 4 ms after stimulation.

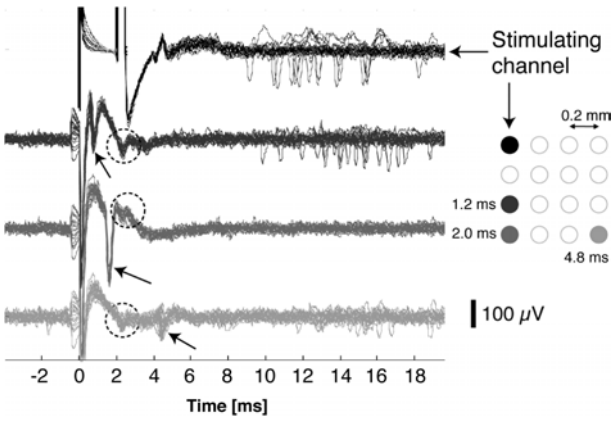

Fig. 15. Recordings through our system with a discharge time of 2 ms @ 50 μA, two pole-shift phases of 2 ms @ 2000 Hz and 0.5 ms @ 500 Hz. Highpass filter setting: 10 Hz. Acquired data were filtered by a digital 2nd order Butterworth highpass filter with a cutoff frequency of 200 Hz. The stimuli were positive-first biphasic pulses with 200 μs per phase, at $\pm$0.5 V. The circles denote additional crosstalk artifacts in the IC, the arrows show time-locked action potentials.

the quality of the neural recording was comparable to the commercial preamplifier system.

Fig. 14 shows the stimulation and recording from the IC. When biphasic voltage pulses (positive–negative, 100 or 500 mV) were applied, artifact-free recordings were possible after 3 $\sim$ 4 ms (or 2 $\sim$ 3 ms if we include the 700-Hz highpass region). By increasing the stimulation intensity, stimulation-induced action potentials appeared around 4 ms. The transient around 3.5 ms is mostly due to the offset step when the highpass filter setting is changed.

Fig. 15 demonstrates the capability of simultaneous multichannel recording and stimulation solely executed by our system. The *stimulating* channel (the topmost trace) recovered from the stimulation artifact as early as 4 ms and recorded diffusive time-locked responses around 10 ms. Nonstimulating channels recovered much earlier from the stimulation artifact (within 500 μs) and recorded highly time-locked action potentials at 1.2, 2.0, and 4.8 ms (the second, third, and fourth traces, respectively).

Although we have made no effort in reducing the artifact in adjacent channels, our previous generation IC was able to record in less than 1 ms, without blanking such channels, after the stimulation (which compares favorably to the adjacent channel performance, with blanking, of the MEA1060BC from MCS). This IC lost some of that capability due to the introduction of crosstalk (the effects of which can be seen in Fig. 15), as the crosstalk from the remaining artifact spike shifts the baseline of the recording channels for 4 ms after stimulation; and it would produce a large stimulation artifact if the channels had not been blanked.

VI. Discussion

We have presented a scalable system built around a custom 16-channel IC that can stimulate and record within 3 ms of the stimulus on the *stimulating* channel and within 500 μs on adjacent channels. We have also demonstrated some of the capabilities of our system for neural culture applications. Our system achieves artifact elimination by directly discharging the electrode through a novel feedback scheme, and by shaping such feedback to optimize electrode behavior; that is, we prevent the problem instead of fighting the consequences. This approach represents a break from existing artifact reduction schemes, in which accumulated electrode charge is not managed thus causing what some researchers call the *dish saturation* effect. This effect makes recording during fast stimulation, or even fast stimulation itself, impossible. An additional benefit of our approach is the increased lifetime of the electrodes, while undischarged electrodes would show variations on their characteristics after a few hours of bipolar stimulation, the use of our artifact elimination protocol allowed us to run the same electrodes continuously for weeks at a time without any appreciable degradation.

The main discharge speed limitation is given by the electrode impedance characteristics [as predicted by Section III-A and (2)]; within this limitation, however, our circuitry is able to reliably control the artifact on the *stimulating electrode* to the point that relatively simple signal processing (e.g., averaging and subtraction or simple filtering) can obtain responses within 3 ms or less. The addition of dynamic bandwidth control further facilitates the achievement of our artifact elimination goal. We have shown how each of the characteristics of the IC interplay with the artifact, and how each of the functions can be used to tune the desired response. Furthermore, we have shown that our design directly affects the electrode by removing the artifact at the source. This effect introduces other design possibilities, such as using the system as a stand-alone stimulator, or independently optimizing the recording and artifact elimination signal paths.

Although we have shown conservative results, and we have not undertaken a careful optimization of our system parameters, we fully expect that better performance will be possible by modifying some of our protocols. Furthermore, given the large number of factors involved, we have strived to provide as much information as possible about the conditions under which artifact elimination is achieved; and to be as precise as possible with

our definitions and terminology thus enabling any future comparisons.

VII. Future Directions

The system is now in use by ourselves and our collaborators in two different laboratories, and the elimination of electrode charge has made possible fast sequential stimulation and recording of neural signals, something that was not possible with existing commercial and custom stimulators. We have shown one example of its use in this paper and we expect other examples to follow as part of additional research. Further work in artifact modeling and characterization is also under way.

Although our system has significantly reduced the artifact duration, we are exploring ways to further improve the performance of our circuitry for the stimulating electrode as well as in the adjacent channels. Through further improvements of our technology, we expect to enable the study of the direct neural responses which have been suggested by [36] and by Fig. 15. Besides correcting some of the shortcomings that have been introduced in the design of the current IC, one such improvement is the use of a negative resistance for R_{disch} to directly reduce the electrode time constant by reducing the effect of R_e. Even with such modifications, we are aware that the system would only be correcting for first order electrode effects; higher order modeling, and a better understanding of the underlying processes, will become necessary to achieve the performance that we seek.

We are in the process of implementing a new IC which will incorporate several improvements in terms of noise performance, bandwidth control, better matching, faster discharge circuitry, and more control for current stimulation. This IC will also incorporate better interfacing characteristics with the full system in mind.

Acknowledgment

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